WHAT IS CLAIMED IS:

1. A modulator comprising:

an offset QPSK modulator, said offset QPSK modulator operative for receiving input data and generating a first output signal representing the modulation to be imposed on a carrier signal to effect offset QPSK modulation of said input signal and a second output signal representing an amplitude of said input data;

a frequency modulator comprising a sigma-delta modulator, said frequency modulator operative for receiving said first output signal generated by said offset QPSK modulator, and generating a control signal representing the desired frequency of said carrier signal such that said carrier signal represents said input signal offset QPSK modulated;

a phase-lock loop circuit comprising a voltage controlled oscillator for generating said carrier signal and a programmable frequency divider, said programmable frequency divider receiving said control signal as an input signal, said programmable frequency divider operative for changing the frequency of the carrier signal in accordance with said control signal, and

an amplifier having variable gain for receiving and amplifying said carrier signal output by said phase-lock loop circuit, said second output signal controlling the amount of gain of said amplifier.

2. A modulator according to claim 1, wherein said offset QPSK modulator comprises:

a demultiplexer for receiving said input data and generating I and Q quadrature signals corresponding to said input data;

a delay circuit operative for receiving said Q quadrature signal from said demultiplexer and for delaying the Q quadrature signal relative to the I quadrature signal;

a digital waveform generator operative for receiving said I quadrature signal output by said demultiplexer and said delayed Q quadrature signal output by said delay circuit, and for generating a digital signal indicating the modulation to be imposed on said carrier signal.

3. A modulator according to claim 2, wherein said offset QPSK modulator further comprises:

a first and second finite impulse response filter coupled to the output of said demultiplexer, said first finite impulse response filter receiving the said I quadrature signal, said second finite impulse response filter receiving said Q quadrature signal, said first and second finite impulse response filters operative for sampling the respective signals at the Nyquist rate.

4. A modulator according to claim 2, wherein said digital waveform generator comprises:

a first lookup table circuit operative for performing an arctangent function, said first lookup table circuit comprising a read-only-memory device, said first lookup table circuit generating a digital output signal indicating the phase of a modulation signal to be imposed on said carrier signal; and

a differentiator coupled to said first lookup table circuit and operative for generating a digital output signal indicating the frequency of said modulation signal to be imposed on said carrier signal.

5. A modulator according to claim 1, wherein said phase-lock loop circuit further comprises:

a reference divider operative for reducing the frequency of a reference signal by a predetermined factor;

a phase detector coupled to said reference divider and said programmable frequency divider, said phase detector operative for generating an error signal indicating the frequency difference between a signal output by said reference divider and a signal output by said programmable frequency divider; and

a filter coupled to the output of said phase detector.

6. The modulator according to claim 1, wherein said control signal is programmable so as to allow said voltage controlled oscillator to be controlled to a desired carrier frequency.

7. The modulator according to claim 2, further comprising a second lookup table for receiving said I quadrature signal and said delayed Q quadrature signal as input signals, and generating an output signal indicating an amplitude of said received I quadrature signal and said delayed Q quadrature signal.

8. The modulator according to claim 1, wherein said carrier signal output by said phase-lock loop circuit has a constant envelope amplitude.

9. The modulator according to claim 1, wherein said amplifier operates to amplitude modulate said carrier signal output by said phase-lock loop in accordance with the value of said second output signal.

10. The modulator according to claim 9, wherein said amplifier outputs a linearized offset QPSK modulated signal.

11. A modulator utilizing direct digital offset QPSK modulation, said synthesizer comprising:

a digital offset QPSK modulator, said digital offset QPSK modulator operative for receiving a digital input data and generating a first digital output signal, said digital output signal representing the modulation to be imposed on a carrier signal to effect offset QPSK modulation of said digital input signal and a second digital output signal representing an amplitude of said digital input data;

a frequency modulator comprising a sigma-delta modulator, said frequency modulator operative for receiving said first digital output signal generated by said digital offset QPSK modulator, and generating a digital control signal representing the desired frequency of said carrier signal such that said carrier signal represents said input signal offset QPSK modulated;

a phase-lock loop circuit comprising a voltage controlled oscillator for generating said carrier signal and a programmable frequency divider, said programmable frequency divider receiving said digital control signal as an input signal, said programmable

frequency divider operative for changing the frequency of the carrier signal in accordance with said control signal; and

an amplifier having a variable gain for receiving and amplifying said carrier signal output by said phase-lock loop circuit, said second digital output signal controlling the amount of gain of said amplifier.

12. A modulator according to claim 11, wherein said digital offset QPSK modulator comprises:

a digital demultiplexer for receiving said input data and generating I and Q quadrature signals corresponding to said input data;

a digital delay circuit operative for receiving said Q quadrature signal from said demultiplexer and for delaying the Q quadrature signal relative to the I quadrature signal;

a digital waveform generator operative for receiving said I quadrature signal output by said digital demultiplexer and said delayed Q quadrature signal output by said digital delay circuit, and for generating a digital signal indicating the modulation to be imposed on said carrier signal.

13. A modulator according to claim 12, wherein said digital waveform generator comprises:

a first lookup table circuit operative for performing an arctangent function, said first lookup table circuit comprising a read-only-memory device, said first lookup table circuit generating a digital output signal indicating the phase of a modulation signal to be imposed on said carrier signal; and

a digital differentiator coupled to said first lookup table circuit and operative for generating a digital output signal indicating the frequency of said modulation signal to be imposed on said carrier signal.

14. The modulator according to claim 12, further comprising a second lookup table for receiving said I quadrature signal and said delayed Q quadrature signal as input signals, and generating an output signal indicating an amplitude of said received I quadrature signal and said delayed Q quadrature signal.

15. The modulator according to claim 11, wherein said carrier signal output by said phase-lock loop circuit has a constant envelope amplitude.

16. The modulator according to claim 1, wherein said amplifier operates to amplitude modulate said carrier signal output by said phase-lock loop in accordance with the value of said second output signal.

17. An offset QPSK modulator comprising:

means for receiving an input data signal to be modulated;

means for generating a digital output signal representing the modulation to be imposed on a carrier signal to effect offset QPSK modulation of said input data signal;

means for generating an amplitude signal indicative of the amplitude of said input data signal;

frequency modulator means for receiving said digital output signal and generating a digital control signal representing the desired frequency of said carrier signal such that said carrier signal represents said input data signal offset QPSK modulated;

means for controlling a programmable frequency divider forming a portion of a phase-lock loop circuit, said programmable frequency divider receiving said digital control signal as an input signal, said programmable frequency divider operative for changing the frequency of said carrier signal in accordance with said control signal, said carrier signal being generated by a voltage controlled oscillator; and

means for amplifying said carrier signal in accordance with the level of said amplitude signal.

18. The offset QPSK modulator according to claim 17, wherein said carrier signal generated by said voltage controlled oscillator circuit has a constant envelope amplitude.

19. The offset QPSK modulator according to claim 17, wherein said digital output signal does not contain amplitude information of said input data signal.

20. The offset QPSK modulator according to claim 17, wherein said amplified carrier signal is a linearized offset QPSK modulated signal.

21. A method for generating an offset QPSK modulated signal at a desired carrier frequency, said method comprising the steps of:

receiving a input data signal to be modulated;

generating a digital output signal representing the modulation to be imposed on said carrier signal to effect offset QPSK modulation of said input data signal;

generating an amplitude signal indicative of the amplitude of said input data signal;

utilizing a frequency modulator comprising a sigma-delta modulator to receive said digital output signal and to generate a digital control signal representing the desired frequency of said carrier signal such that said carrier signal represents said input signal offset QPSK modulated;

controlling a programmable frequency divider forming a portion of a phase-lock loop circuit, said programmable frequency divider receiving said digital control signal as an input signal, said programmable frequency divider operative for changing the frequency of said carrier signal in accordance with said control signal, said carrier signal being generated by a voltage controlled oscillator; and

amplifying said carrier signal in accordance with the level of said amplitude signal.

22. A method for generating an offset QPSK modulated signal at a desired carrier frequency according to claim 21, further comprising the steps of:

demultiplexing said input data signal and generating digital I and Q quadrature signals corresponding to said input data signal;

delaying the Q quadrature signal relative to the I quadrature signal;

performing an arctangent function on said delayed Q quadrature signal and said I quadrature signal so as to generate an output signal indicating the phase of a modulation signal to be imposed on said carrier signal; and

differentiating said output signal so as to generate a digital signal indicating the frequency of said modulation signal to be imposed on said carrier signal.

23. A method for generating an offset QPSK modulated signal at a desired carrier frequency according to claim 21, wherein said digital control signal is programmable so as to allow said voltage controlled oscillator to be controlled to a desired carrier frequency.

24. A method for generating an offset QPSK modulated signal at a desired carrier frequency according to claim 21, wherein said carrier signal output by said phase-lock loop circuit has a constant envelope amplitude.

25. A method for generating an offset QPSK modulated signal at a desired carrier frequency according to claim 21, wherein said carrier signal output by said phase-lock loop is amplitude modulated in accordance with the value of said amplitude signal.

26. A method for generating an offset QPSK modulated signal at a desired carrier frequency according to claim 25, wherein said amplitude modulated carrier signal is a linearized offset QPSK modulated signal.

27. A vector modulator comprising:

means for receiving an input data signal to be modulated;

means for generating a digital output signal representing the modulation to be imposed on a carrier signal to effect quadrature modulation of said input data signal;

means for generating an amplitude signal indicative of the amplitude of said input data signal;

frequency modulator means for receiving said digital output signal and generating a digital control signal representing the desired frequency of said carrier signal such that said carrier signal represents said input data signal quadrature modulated;

means for controlling a programmable frequency divider forming a portion of a phase-lock loop circuit, said programmable frequency divider receiving said digital control signal as an input signal, said programmable frequency divider operative for

changing the frequency of said carrier signal in accordance with said control signal, said carrier signal being generated by a voltage controlled oscillator; and

means for amplifying said carrier signal in accordance with the level of said amplitude signal.

28. A vector modulator comprising:

a quadrature modulator, said quadrature modulator operative for receiving input data and generating a first output signal representing the modulation to be imposed on a carrier signal to effect quadrature modulation of said input signal and a second output signal representing an amplitude of said input data;

a frequency modulator comprising a sigma-delta modulator, said frequency modulator operative for receiving said first output signal generated by said quadrature modulator, and generating a control signal representing the desired frequency of said carrier signal such that said carrier signal represents said input signal quadrature modulated;

a phase-lock loop circuit comprising a voltage controlled oscillator for generating said carrier signal and a programmable frequency divider, said programmable frequency divider receiving said control signal as an input signal, said programmable frequency divider operative for changing the frequency of the carrier signal in accordance with said control signal, and

an amplifier having variable gain for receiving and amplifying said carrier signal output by said phase-lock loop circuit, said second output signal controlling the amount of gain of said amplifier.